Amirhossein Azarabadi

Contact Information

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Education

Ph.D. in *Computer Science* (GPA: 3.89) Advisor: Prof. Lennart Johnsson
High-performance Computing, Re-configurable Systems, FPGA Design
Department of Computer Science, University of Houston Sep. 2019 - Present

B.Sc. in *Computer Engineering* GPA: 16.38 (2nd rank)
FPGA Design and Computer Architecture
Shahid Beheshti University, Tehran, Iran Sept. 2014 - July 2019

Work Experience

Research Assistant Fall 2019 - Present
University of Houston, Advisor: Prof. Lennart Johnsson
My research focused on energy-efficient computing and computer architecture design. I am currently working on Intel Movidius Myriad 2 Vision Processing Unit (VPU) trying to make matrix multiplication more efficient by using different strategies and algorithms.

Hardware Design Member Spring 2018 - Spring 2019
Green IoT Lab
A research member of Green IoT lab under the supervision of Dr. Attarzadeh-niaki. My research focused on the implementation of efficient IoT devices with different frameworks (Using VHDL and embedded system software programming in C/C++).

Hardware Design Intern Spring 2018 - Fall 2018
Novin Tarasheh Alborz
The research focused on designing and implementation a sound source localization system using a microphone array on a MAX10 FPGA (B.Sc. project). My responsibilities involved gathering data by using the ADC module from round-shapes microphones and using different methods and algorithms to process signals and localize the sound source. Besides, designing efficient hardware with different architectures to process data by using VHDL and implementing signal processing algorithms in C++.

Hardware Design Intern Summer 2017 - Spring 2018
Nik Fanavaran Plasma
The research focused on the optimization of biomedical devices and reducing system noise with hardware techniques. My responsibilities involved assembling circuit components and analyzing the circuits by circuit analysis tools (oscilloscope and multi-meter). Also, I was working on analyzing and simulating circuits with PSpice and compare simulations with real-world data.

Technical Skills

Technical Knowledge
Re-configurable Systems and Computer Architecture, Behavioral Design and verification, RTL and structural Design and verification, Embedded Systems Hardware and Software, Internet of Things, High-performance Computing, Design and implement hardware components, Simulate the performance and capacity of HDL codes, Ability to program a variety of FPGAs and using different features and IPs, Programming microprocessors and using different modules, Analyzing circuits

Hardware Design
Verilog, VHDL, Qsys, Behavioral Design, RTL and structural Design, Synopsys Design Vision, HLS

FPGAs
Intel MAX, Intel Cyclone IV and V, Xilinx Spartan

Programming Languages and Scripting
C, C++, Python, Java, Matlab, Bash, Slurm

Micro Controllers
Intel Movidius Myriad 2, ARM, AVR, Raspberry Pi

Simulation and Design Software
ISE Modelsim, Proteus, Quartus, Simulink

Parallel Programming and Profiling Tools
OpenMP, OpenACC, TAU

Circuit Analysis Tools
PSpice, HSpice

Selected Projects

Re-configurable Systems and Hardware design

- **Design and Implementation of a Sound Source Localization System Using a Microphone Array on a MAX10 FPGA — B.Sc. Project** 2018
  This project focused on the design of a sound source localization system by using 6 microphones in a round shape panel. The signal processing part was done by a MAX 10 NEEK platform using NIOS II soft processors. All microphones were sampled at 100 kHz using a MAX 10 ADC and the stored data was processed to determine the difference between Times of Arrivals (ToAs). The application of this work is in calculating the exact position of a sound source. Designing the hardware part and software code was done by myself under the supervision of Dr. Attarzadeh-niaki.

- **SBU-cordic Design** 2019
  Implementation of Codric algorithm. The code was written in VHDL and the layout was designed by Synopsys design vision. My responsibilities involved writing the Cordic code and generating layout by Synopsys and implementing optimization techniques for reducing the area and energy consumption.

- **SBU-processor and Mano CPU** 2016
  Design and implementation of an 8 bit, five stages pipelined microprocessor for SBU-processor (using Verilog). My responsibilities involved implementation and simulation of Mano CPU with two levels memory hierarchy storage system (cache and main memory) using an HDL (using VHDL and Design Vision for implementation and ISE Modelsim for simulation).

Internet of Things and Embedded Systems

- **Motion Detector** 2020
  Design and implementation of a motion detector for biomedical purposes (using Raspberry Pi). My responsibilities involved implementing hardware and writing code by using the delta-sigma algorithm (Embedded C++ programming).

- **Smart Insulin Injection Pen** 2017
  Design and fabrication of smart insulin injection pens with smartphone connection feature (using ARM microprocessor). Designing the hardware by using a WIFI transceiver wireless module and a stepper motor. My responsibilities involved designing hardware and writing software parts using embedded C++.

High-performance Computing

- **Parallelized Quickselect on Distributed Nodes** 2019
  Implementation and optimization of Quickselect (C++) on distributed nodes by OpenMP. My responsibilities involved the implementation of the Quickselect algorithm on distributed nodes using OpenMPI and gathering data and analyzing results.

Miscellaneous

- **Instructions Set Simulator (ISS)** 2020
  Designing a simulator for a 16-bit microprocessor and it provides a virtual platform for system emulation. It provides real-time states of registers, components, and details about each step of the code. My responsibilities involved designing the platform based on the instruction set and implementation of the real-time simulator. (Using C++)

- **SBU-wireless Network Player** 2016
  Design and programming of a network-based player with the ability of playing a song by up to 10 connected devices (using Java)